

Amendment to the Claims

29. (CURRENTLY AMENDED) A stacked-gate flash memory having a shallow trench isolation with a high-step oxide and high lateral coupling comprising:

a substrate having a ~~gate oxide layer~~ surface;

at least two trenches, each of said trenches formed in said surface of said substrate to a depth between about 2500 to 5000 Å below the surface of said substrate;

an oxide layer conformally formed over on the walls and bottom of each said trench, ~~said substrate, including over the inside walls of said two trenches~~;

a high-step oxide formed over said oxide layer within said ~~two trenches~~ over said oxide layer and protruding vertically upward over the from said surface of said substrate to a height between about 2000 to 6000 Å;

~~said high step oxide forming an opening with high walls over the surface of said substrate between said two trenches~~;

a contiguous pair of said high-step isolation oxides forming an opening in the space over said surface of said substrate between said pair of high-step isolation oxides, said opening having vertical interior walls;

a gate oxide formed on said surface of said substrate between said contiguous pair of said high-step isolation oxides;

~~a first conductive layer formed conformally inside and extending above said opening and over the surface of the substrate between said high walls to form a floating gate having internal and external folding surfaces;~~

a first conductive layer formed conformally on said gate oxide within said opening and on said interior walls of said opening and extending above said opening, said first conductive layer having an interior surface within the opening, said first conductive layer having internal, external and top surfaces above said opening, said first conductive layer functioning as a floating gate residing completely within said opening;

~~an intergate oxide layer formed over said internal and external folding surfaces of said floating gate;~~ conformally formed over said external, top and internal surfaces of said first conductive layer, said intergate oxide layer thus having external, top and internal surfaces;

a second conductive layer formed over said intergate oxide layer protruding downward in between said internal and external folding surfaces over of said intergate oxide layer, said second conductive layer forming to form a control gate having high lateral coupling with said floating gate; and .

a self-aligned source ~~-(SAS)-~~line.

33. (CURRENTLY AMENDED) The stacked-gate flash memory cell of claim 29, wherein said opening has a width between about 1500 to ~~3-5000~~ 5000 Å.

34. (PREVIOUSLY PRESENTED) The stacked-gate flash memory cell of claim 29, wherein said first conductive layer is polysilicon having a thickness between about 100 to 500 Å.

35. (PREVIOUSLY PRESENTED) The stacked-gate flash memory cell of claim 29, wherein said second conductive layer is polysilicon having a thickness between about 1000 to 3000 Å.